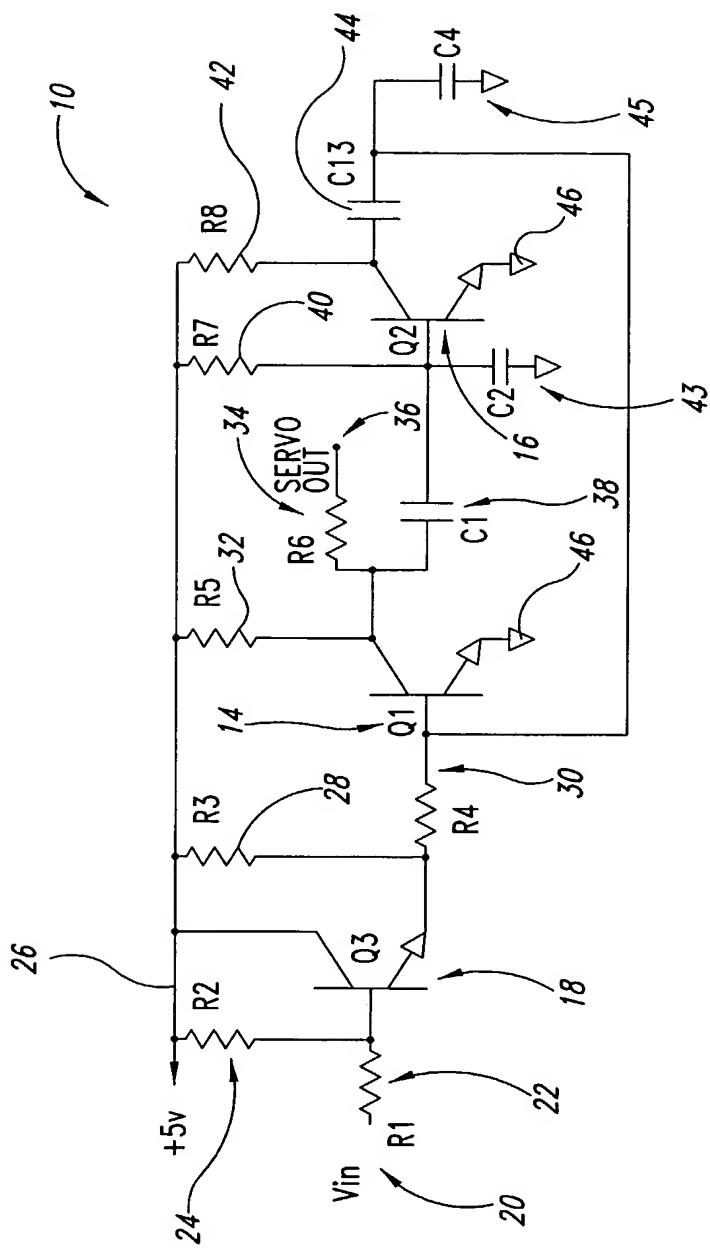


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BASIC MOTOR NEURON CIRCUIT

FIG. 1

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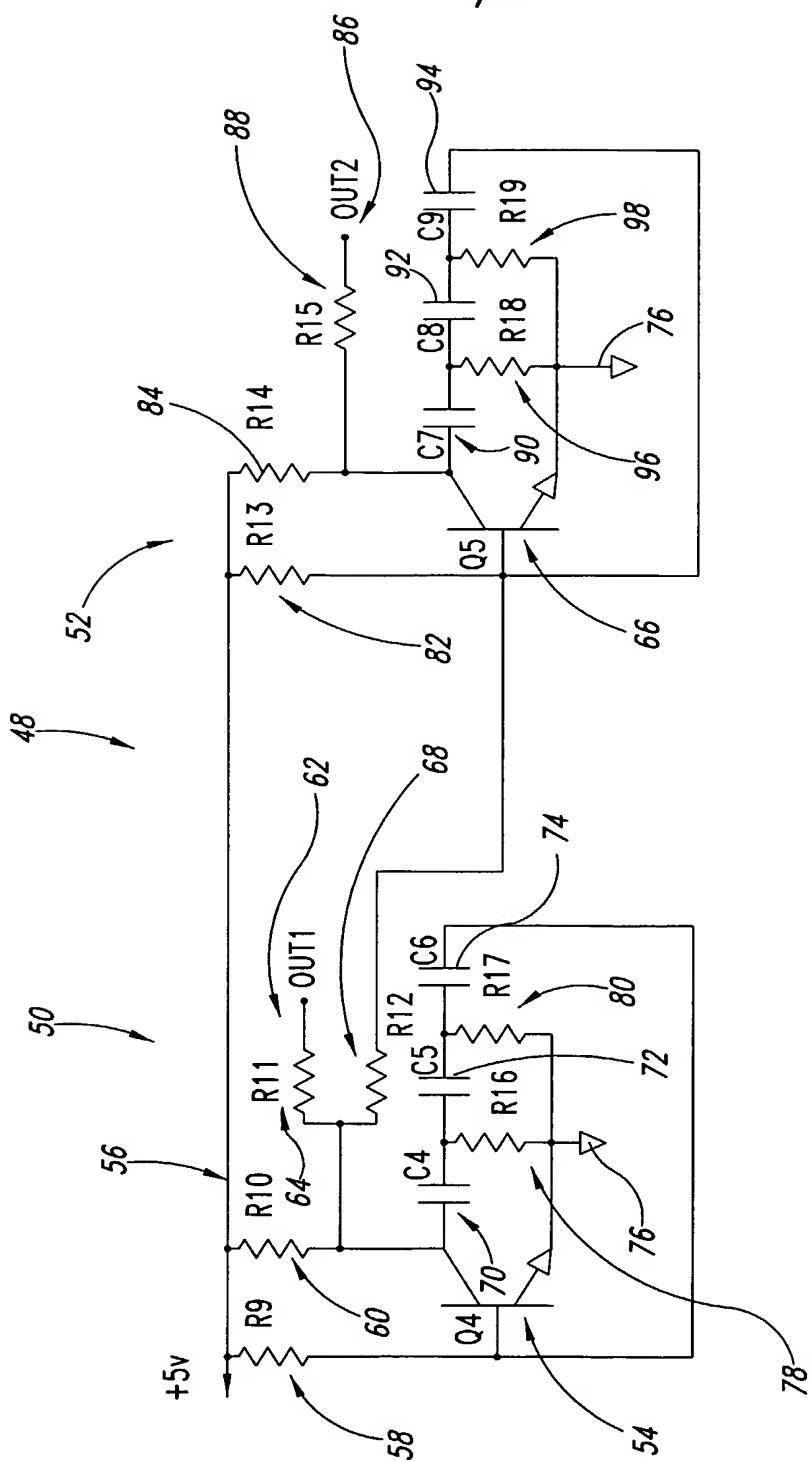


FIG. 2

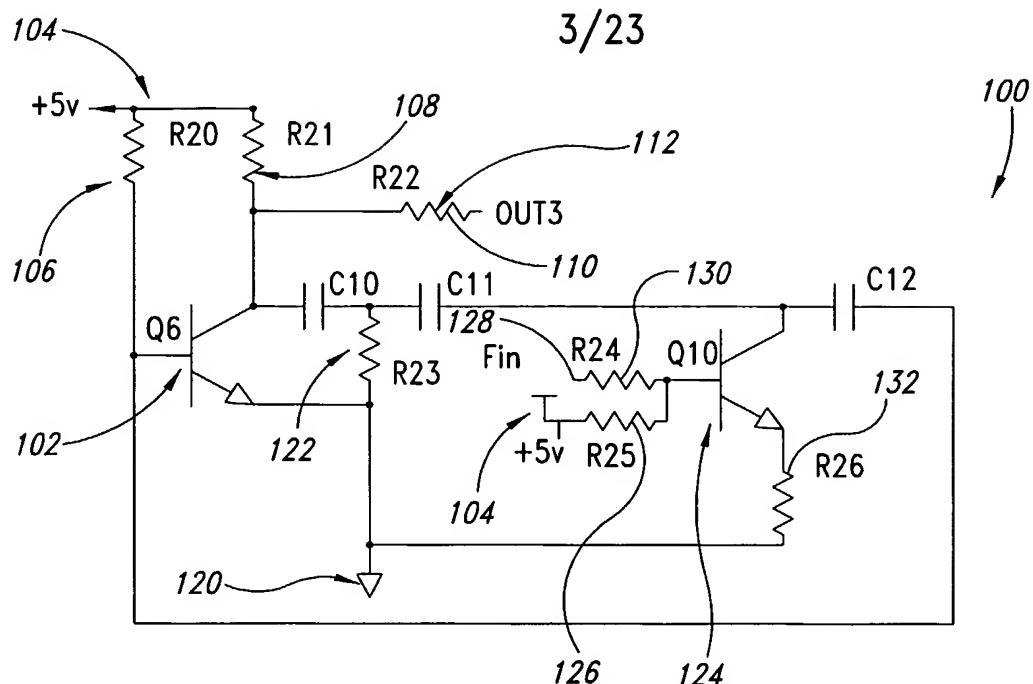


FIG. 3

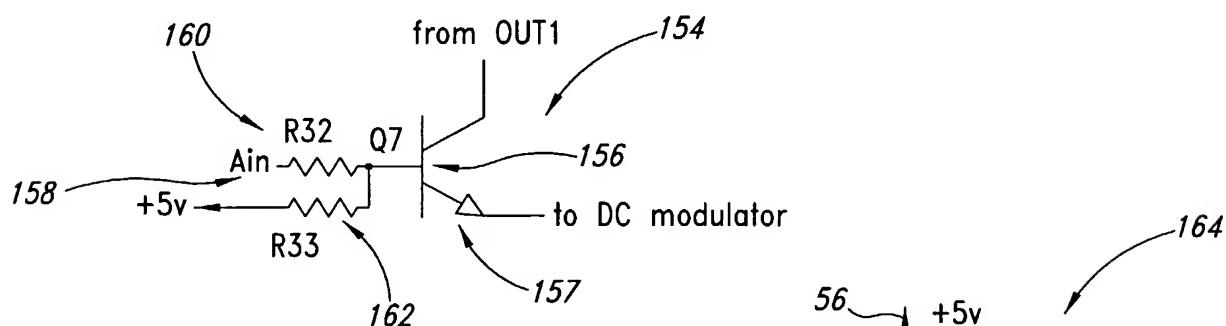


FIG. 5

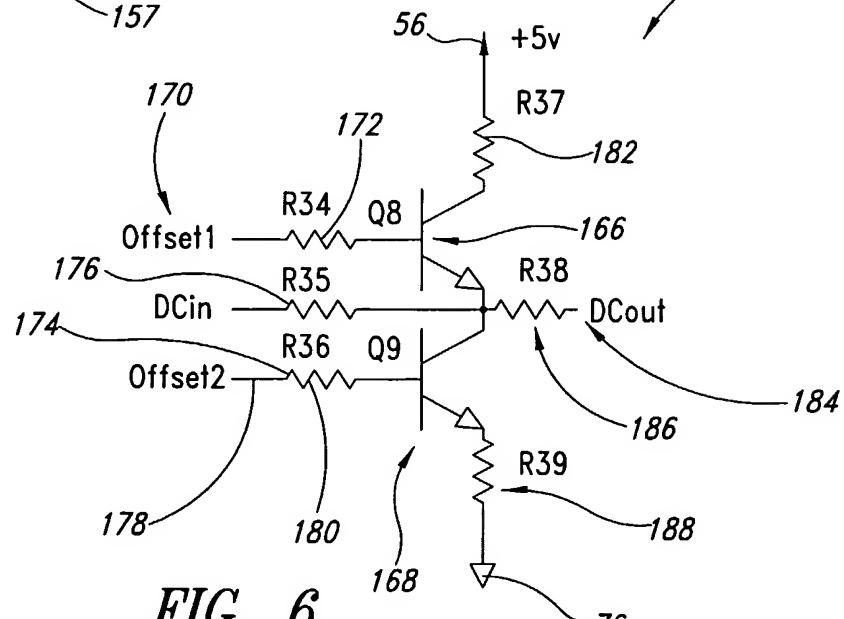


FIG. 6

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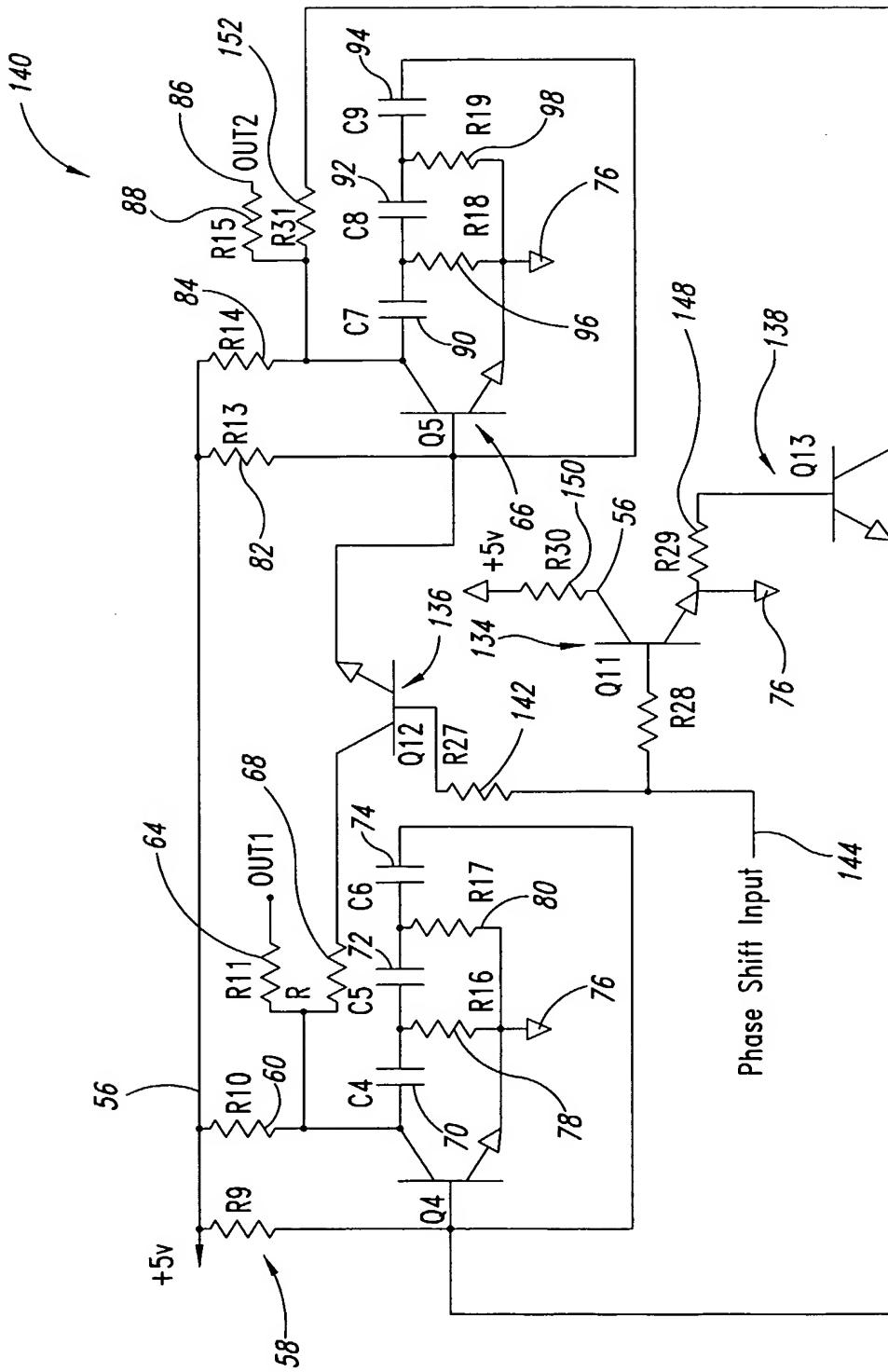


FIG. 4

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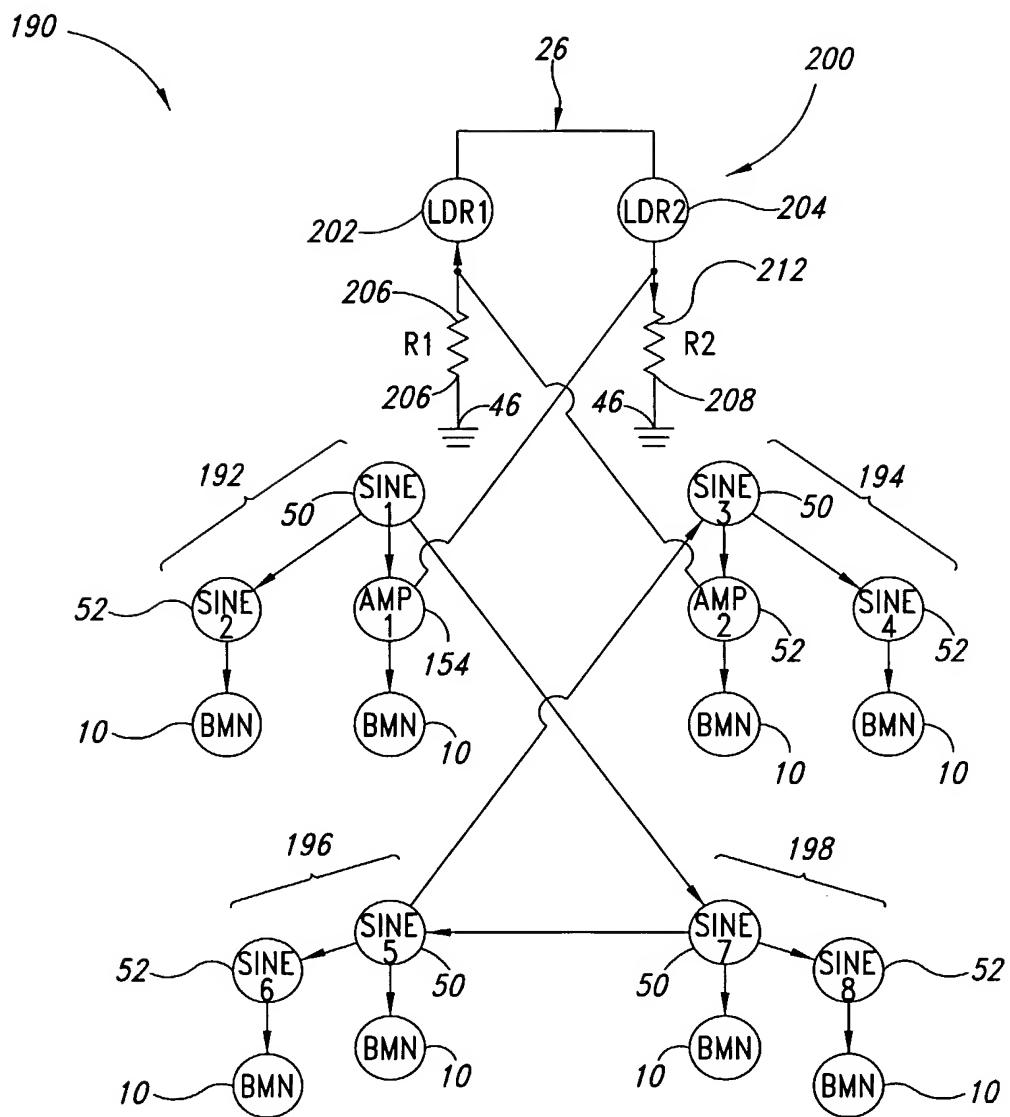


FIG. 7

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SYNTHETIC NERVOUS SYSTEM TOPOLOGY

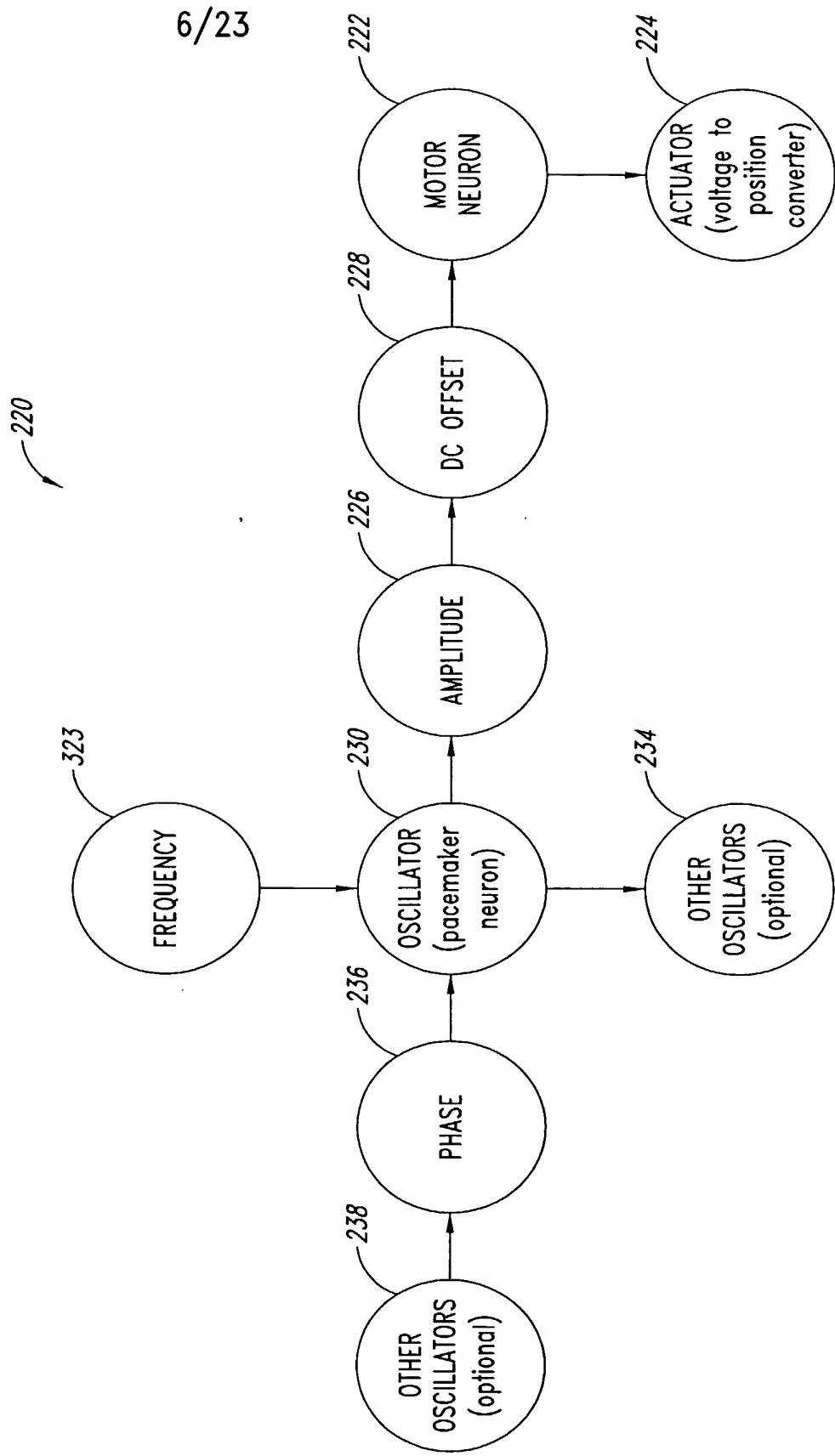


FIG. 8

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555 TIMER AS A MOTOR NEURON

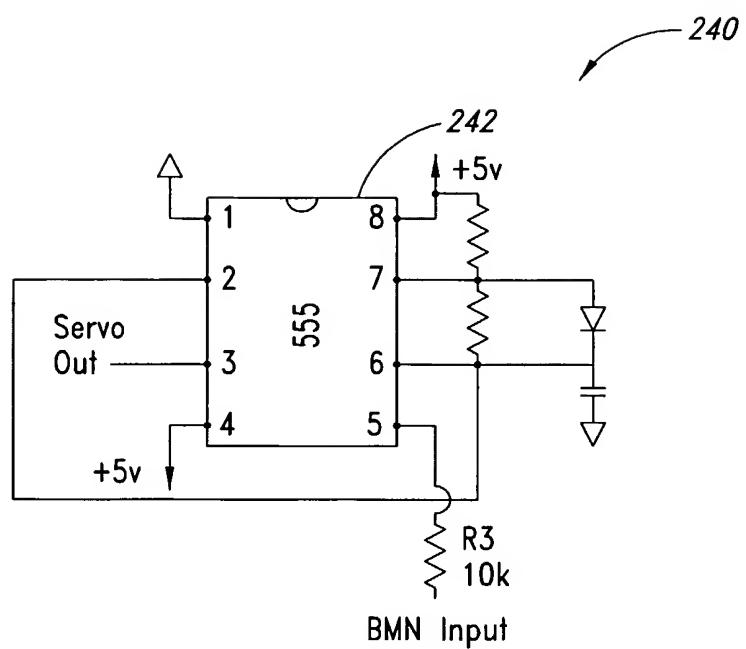


FIG. 9

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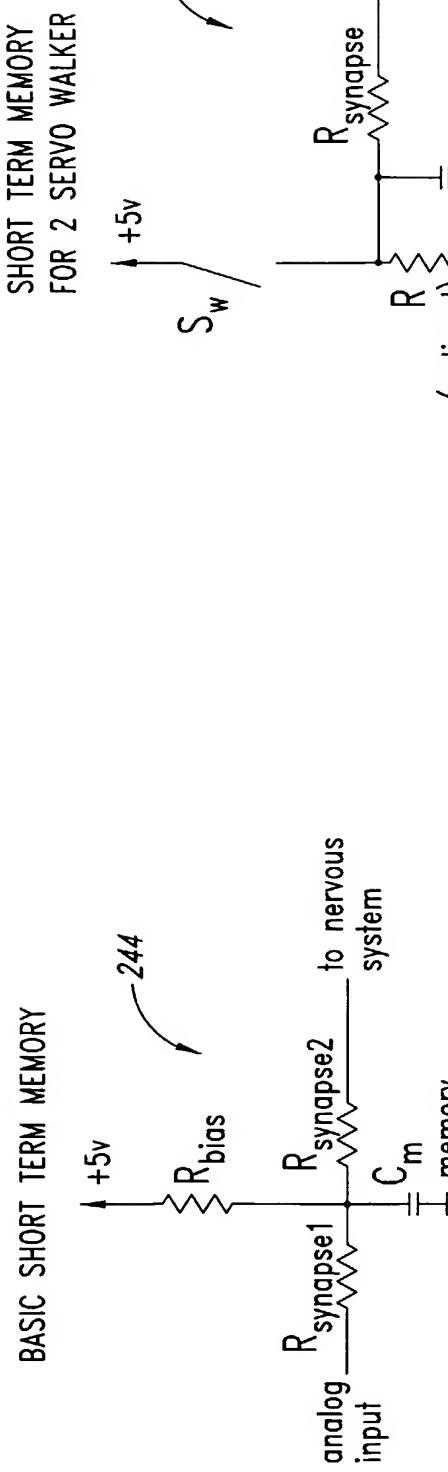


FIG. 10A

SIMPLE ANALOG INPUT
TO SHORT TERM MEMORY

FIG. 10B

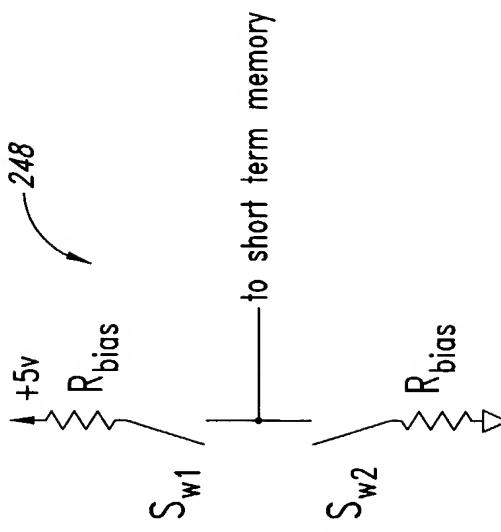


FIG. 10C

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NE567 TONE DECODER/PHASE-LOCKED LOOP AS A
TIGHTLY COUPLED CENTRAL PATTERN GENERATOR

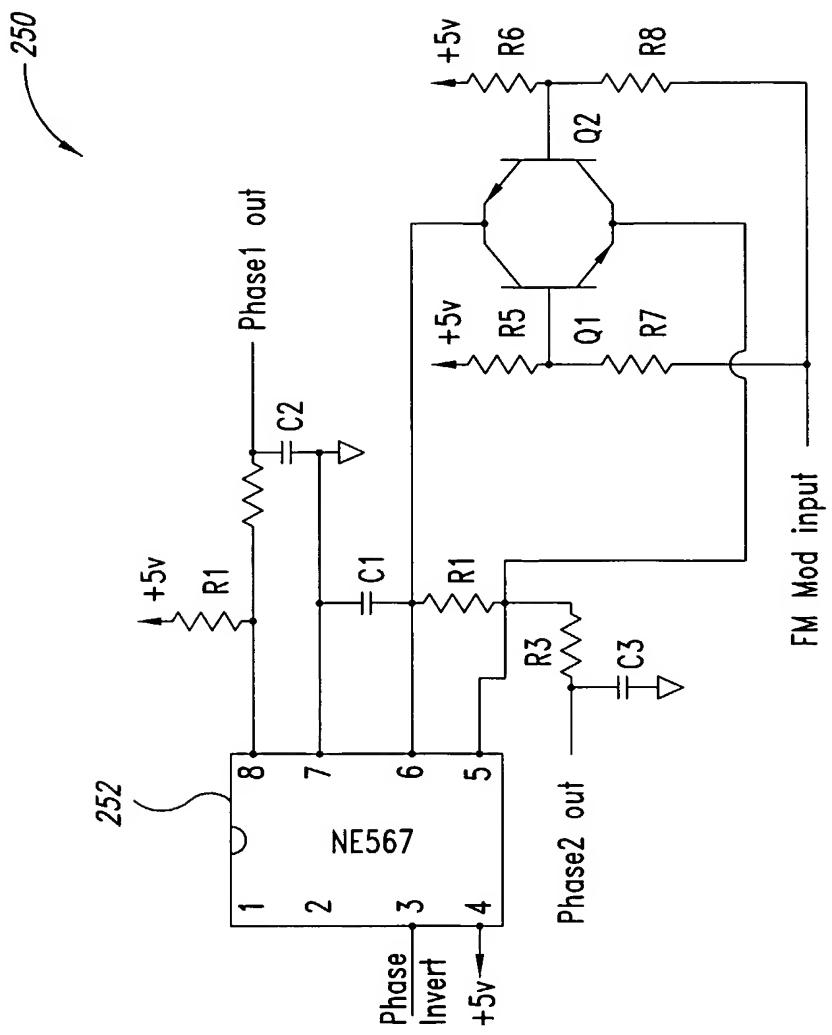


FIG. 11

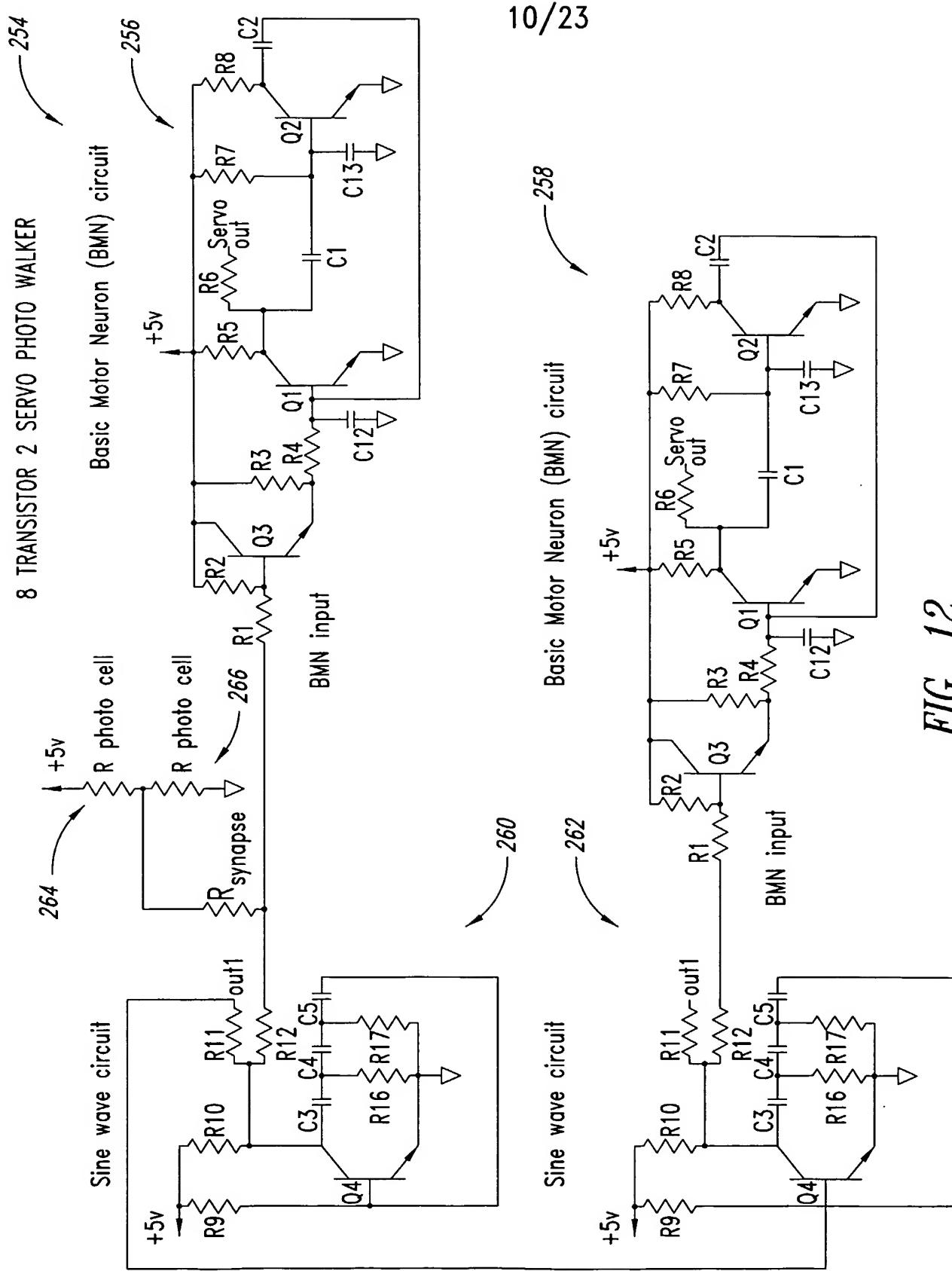


FIG. 12

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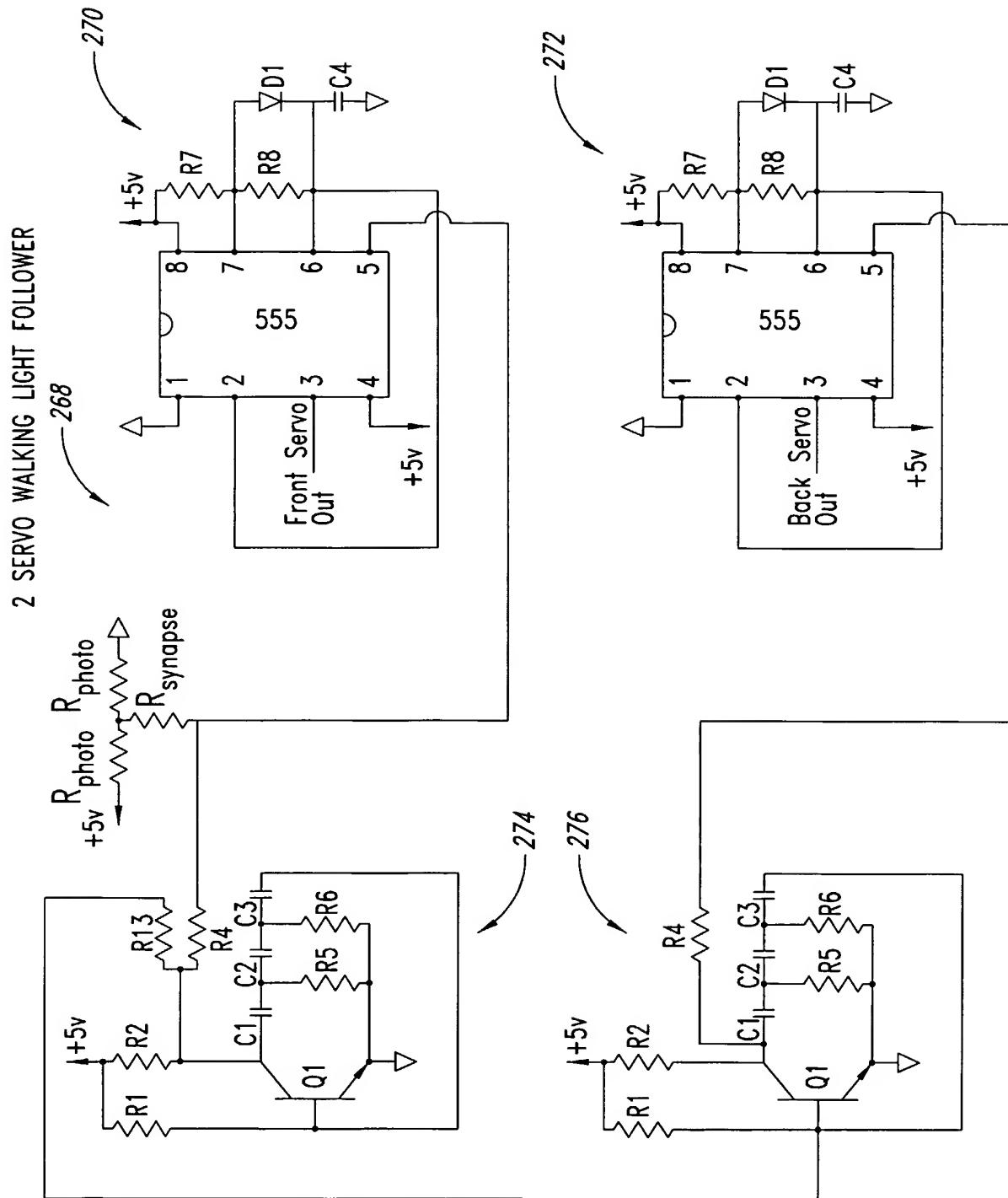


FIG. 13A

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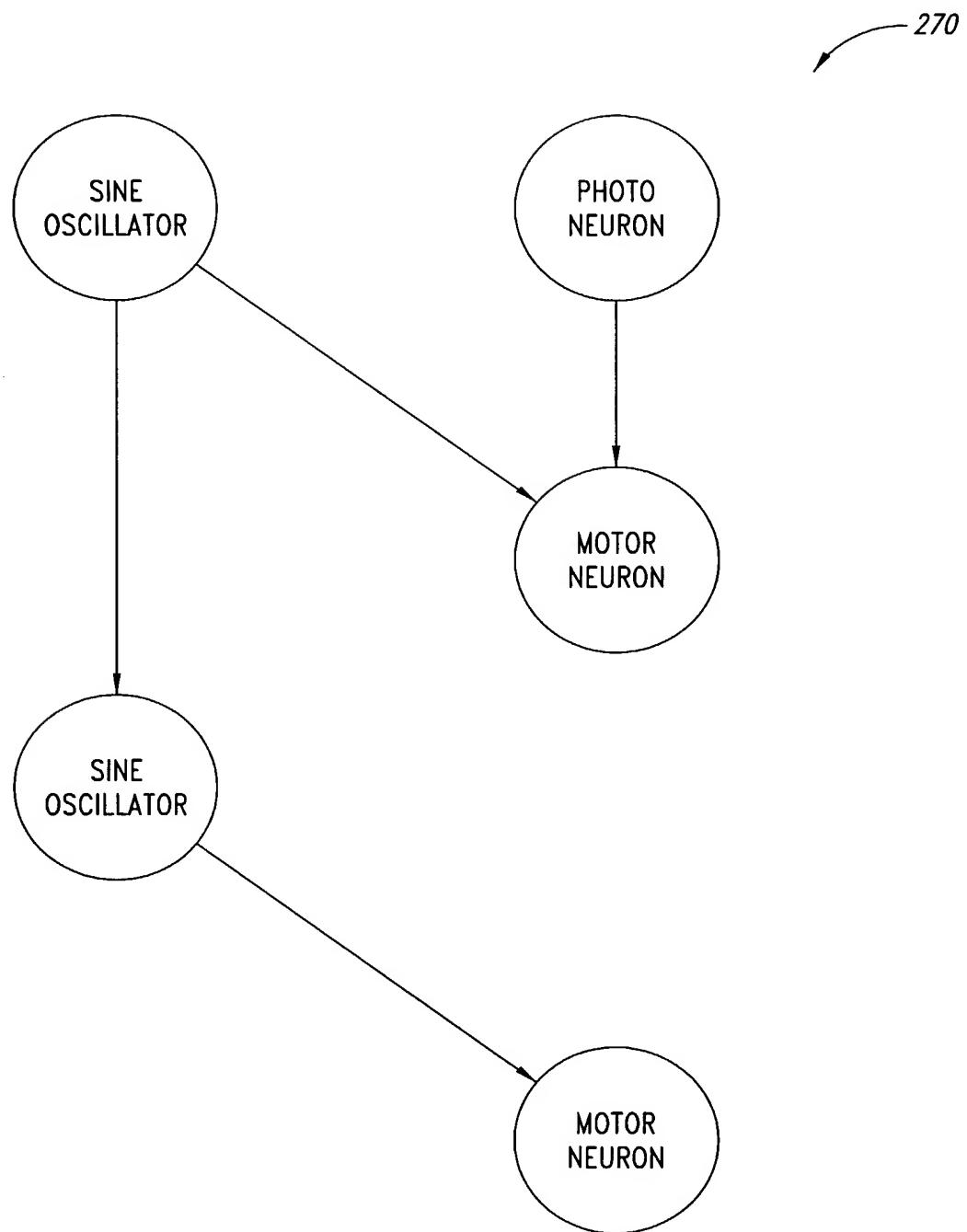


FIG. 13B

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PHASE SWITCH MATRIX WITH QUADPOD

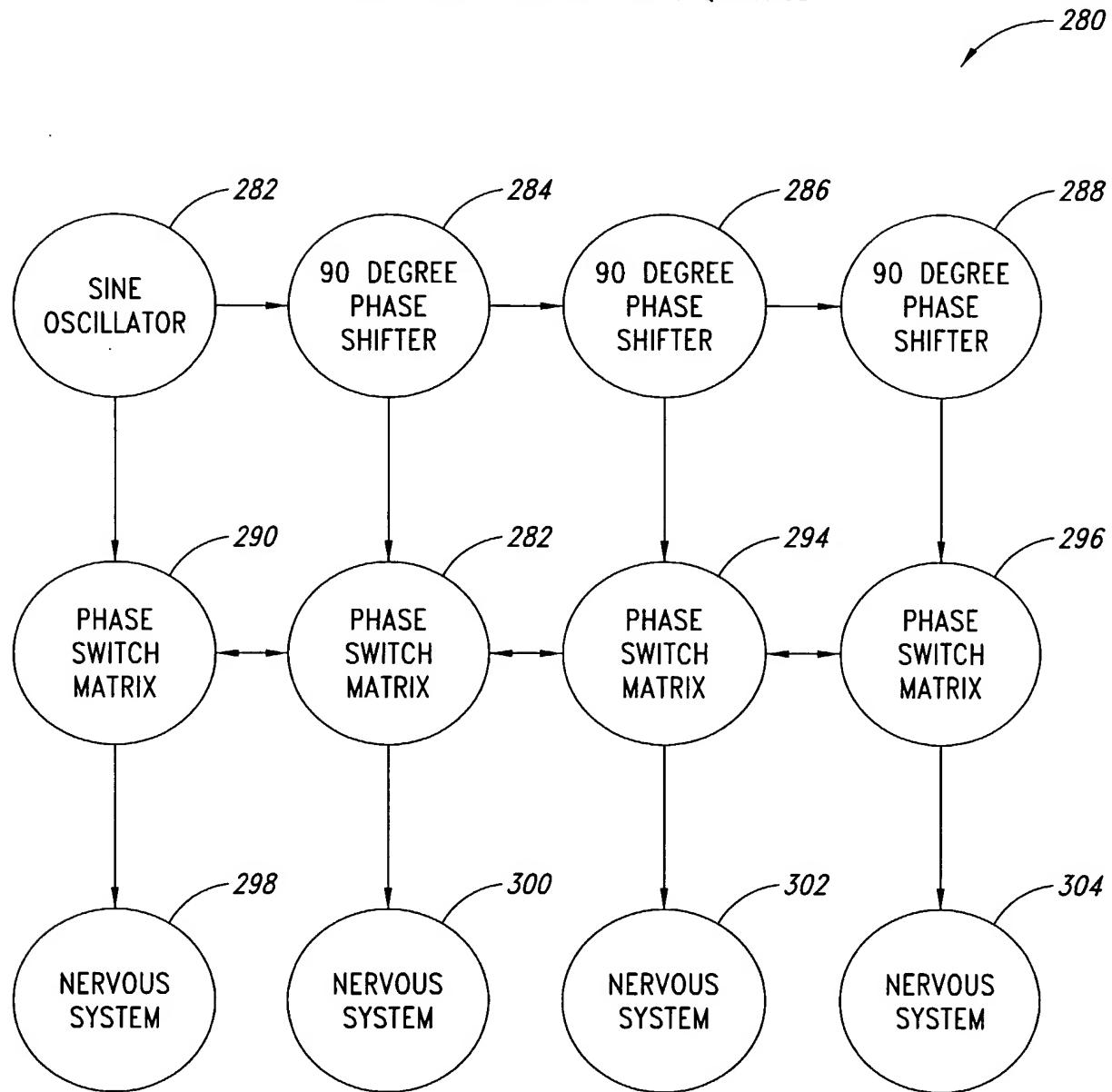
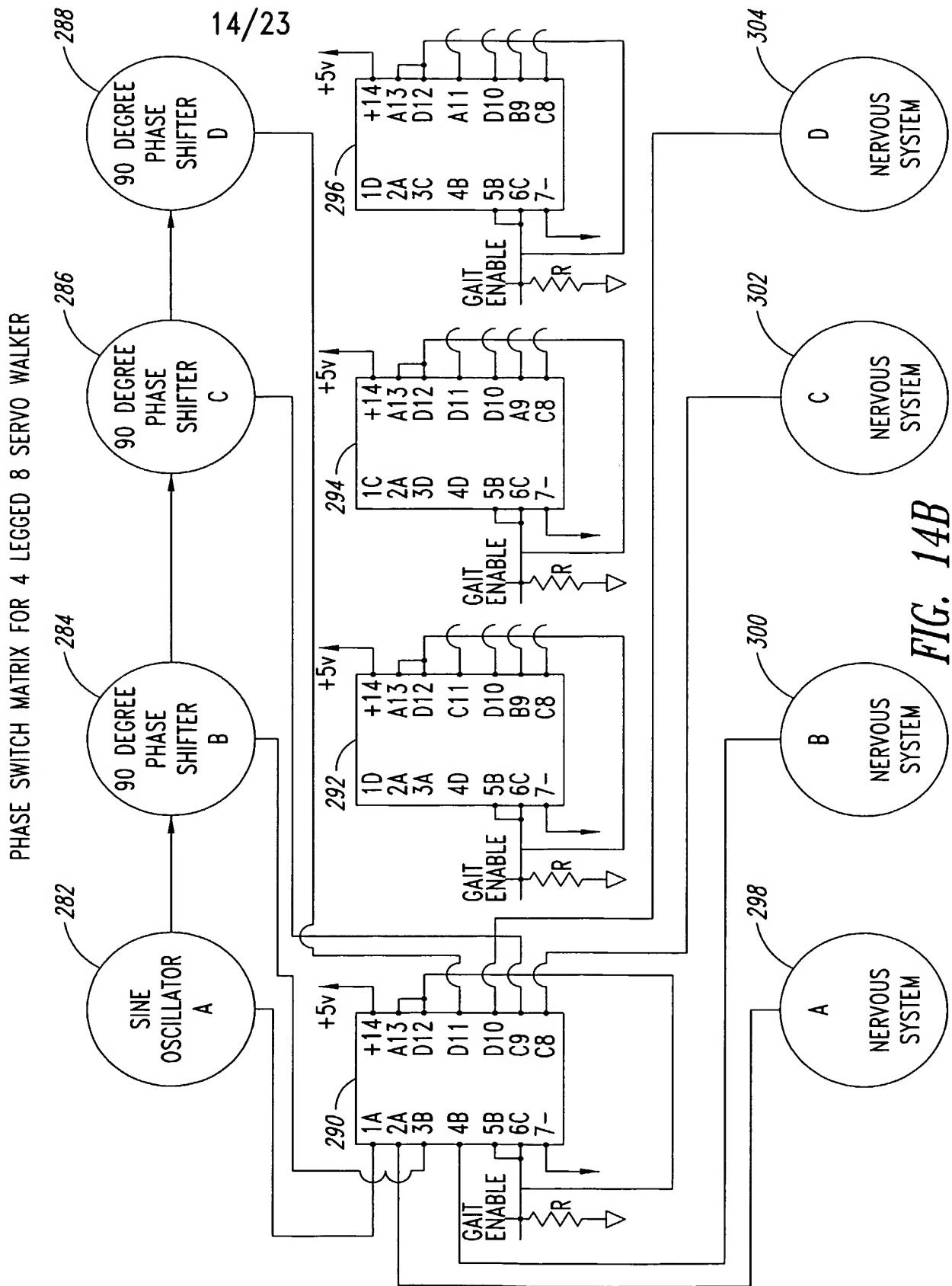


FIG. 14A



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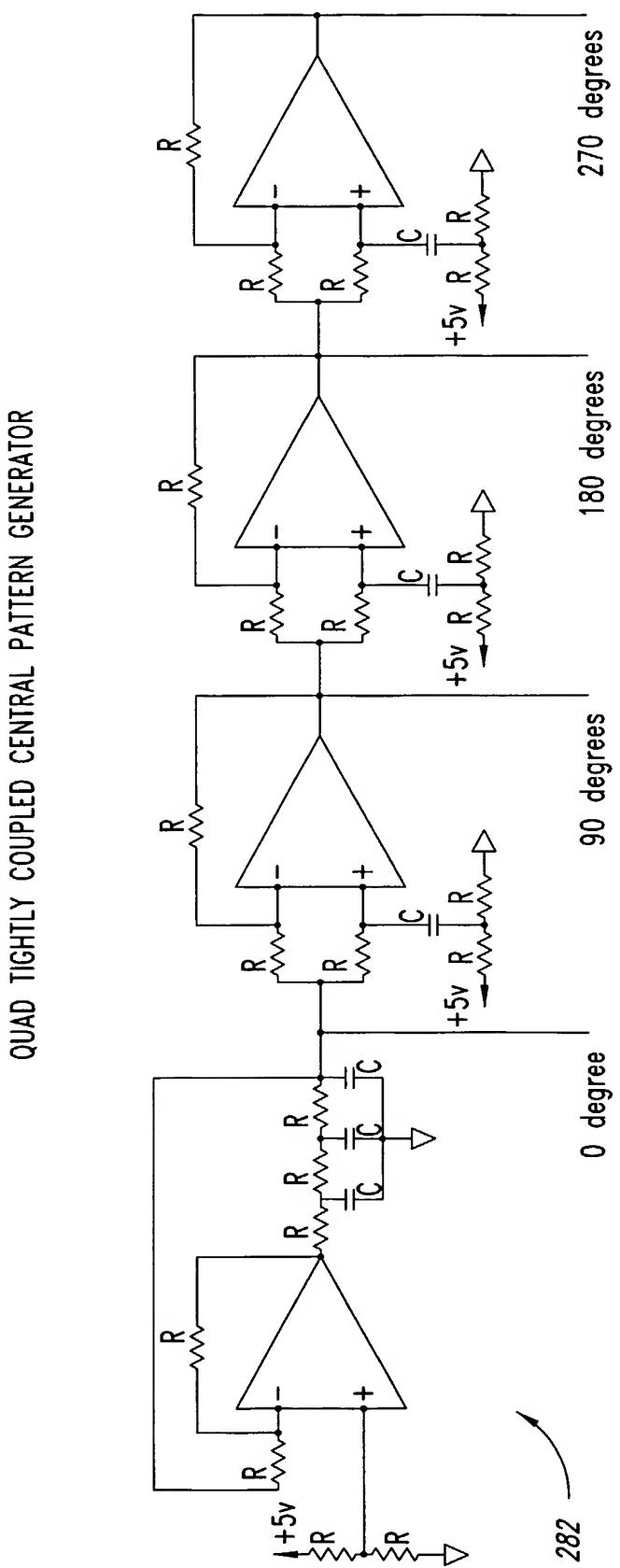


FIG. 14C

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voltage to position converter

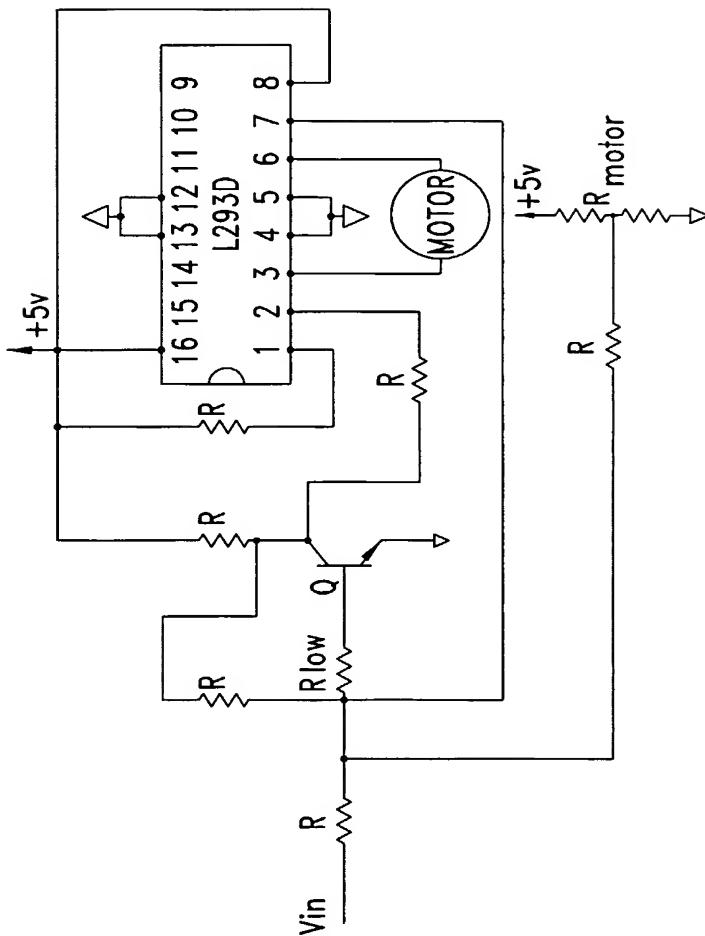


FIG. 14D

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LEARNING CONNECTIONIST SYNAPSE

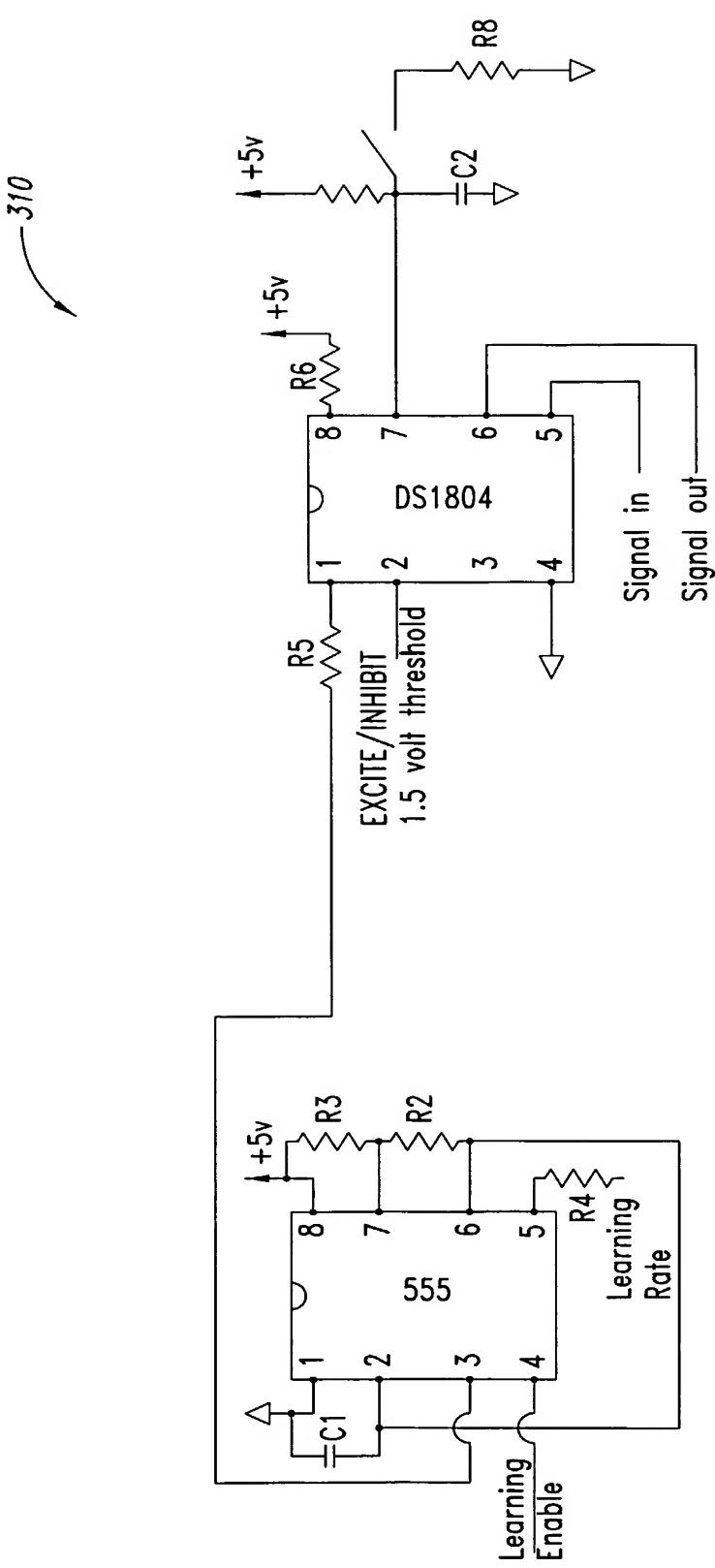


FIG. 15A

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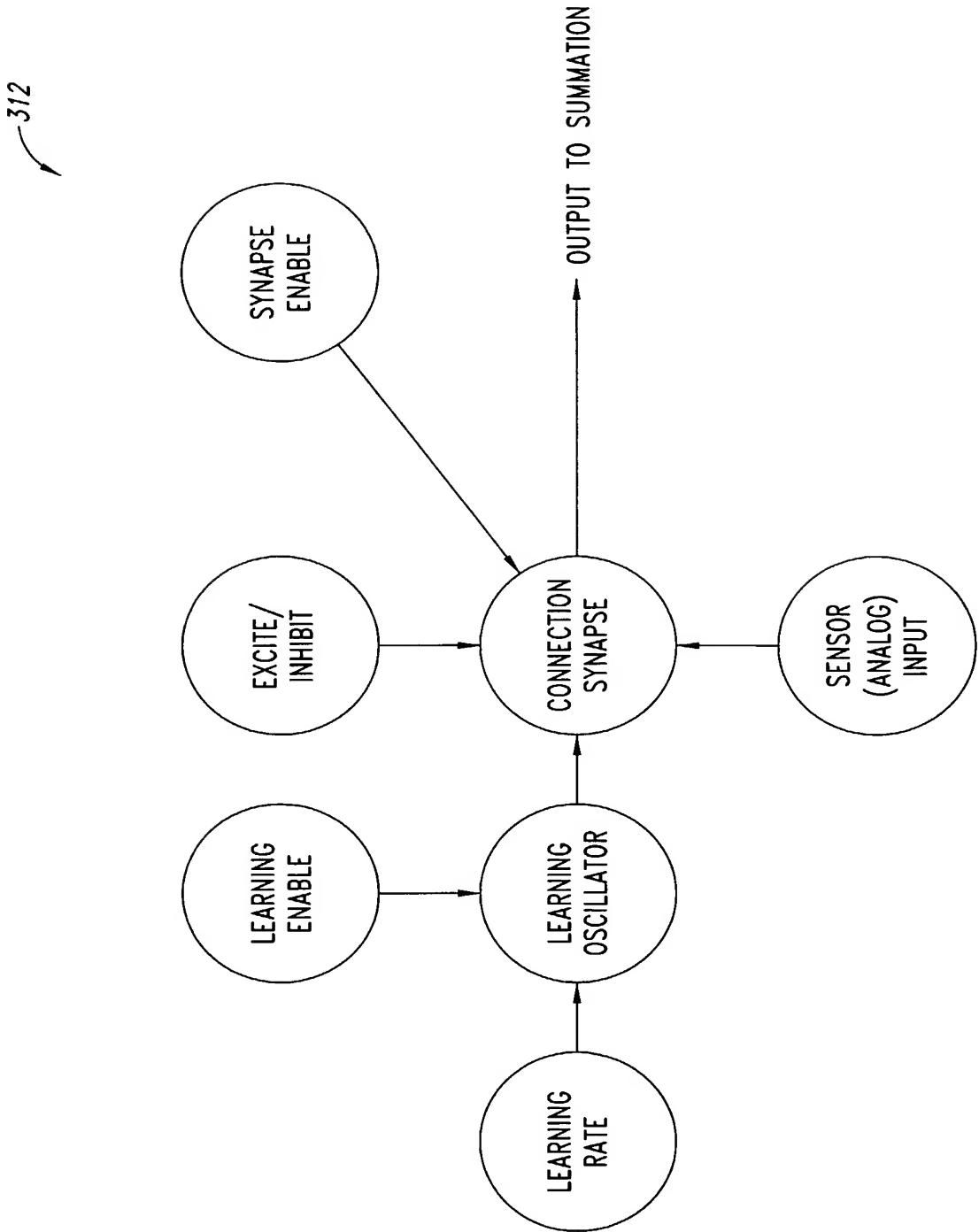


FIG. 15B

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LEARNING CONNECTIONIST NEURON

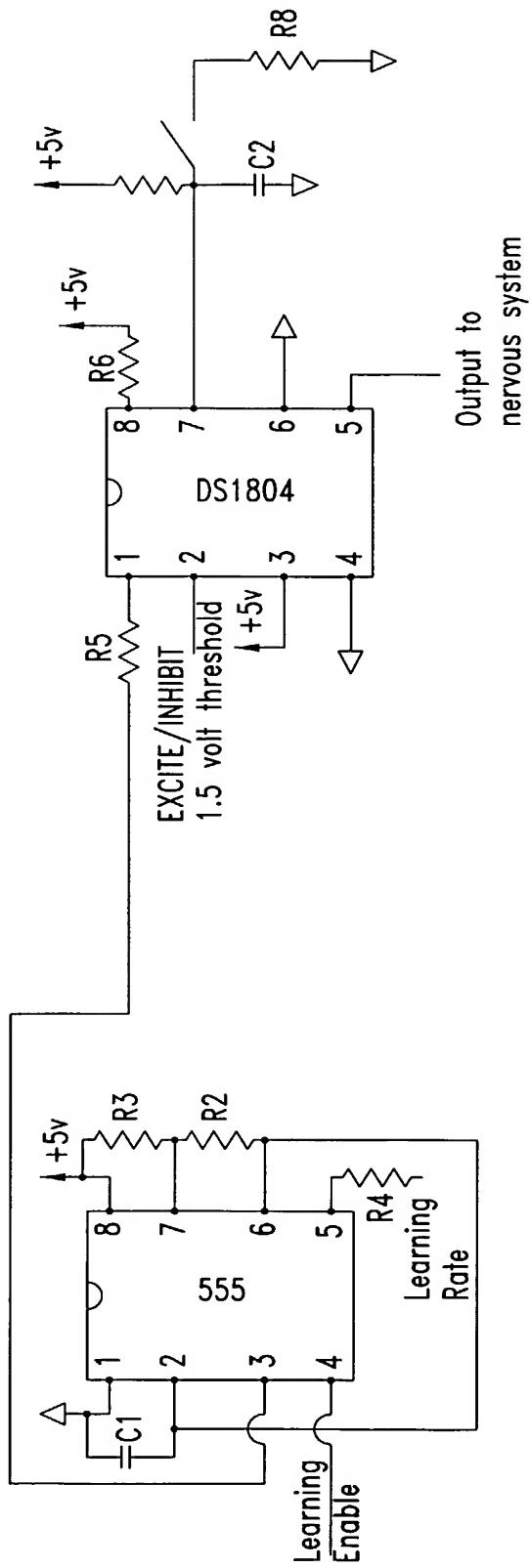


FIG. 16A

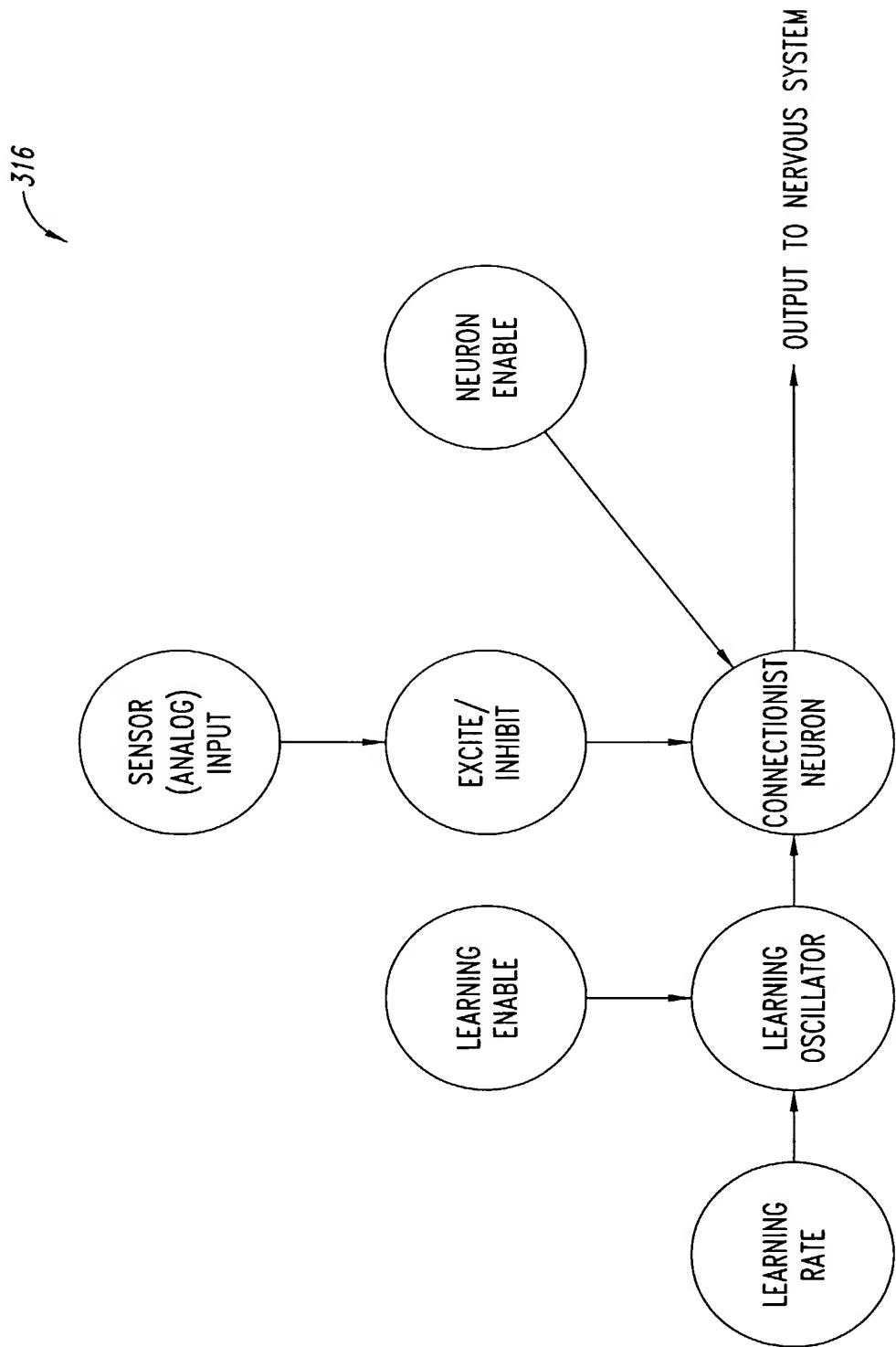


FIG. 16B

EXAMPLE 3 INPUT SYNAPSE ARRAY

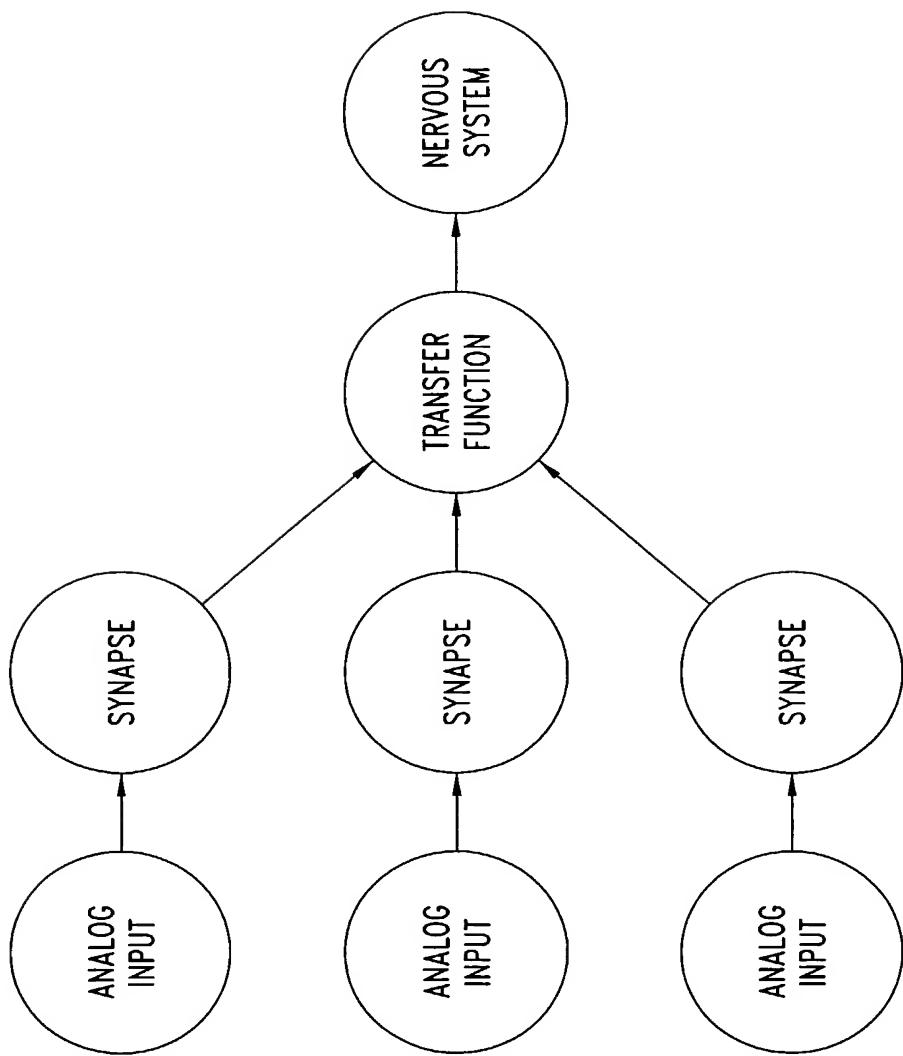


FIG. 17

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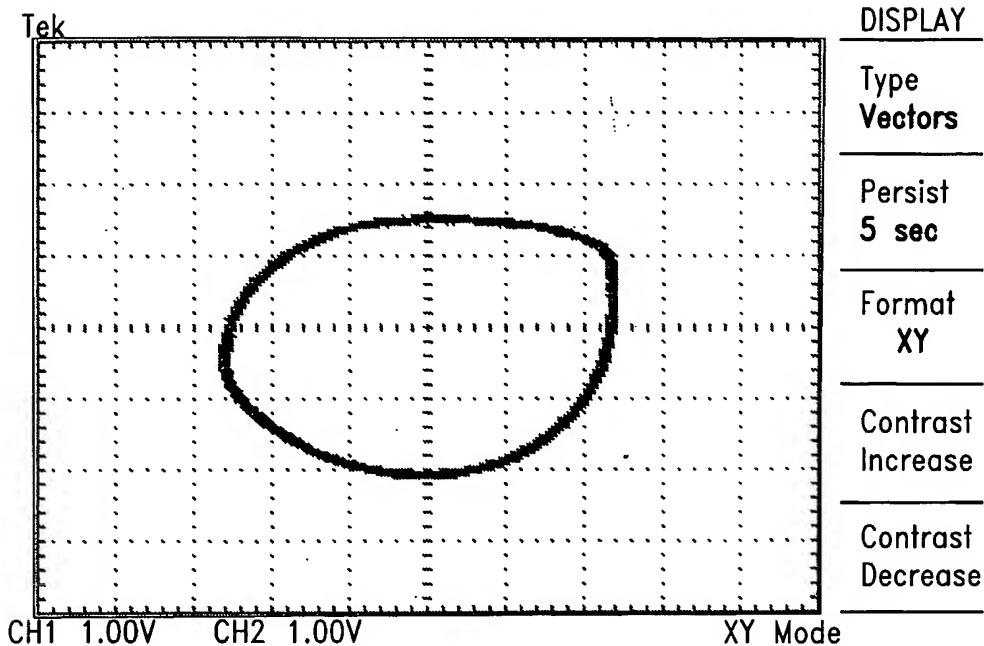


FIG. 18

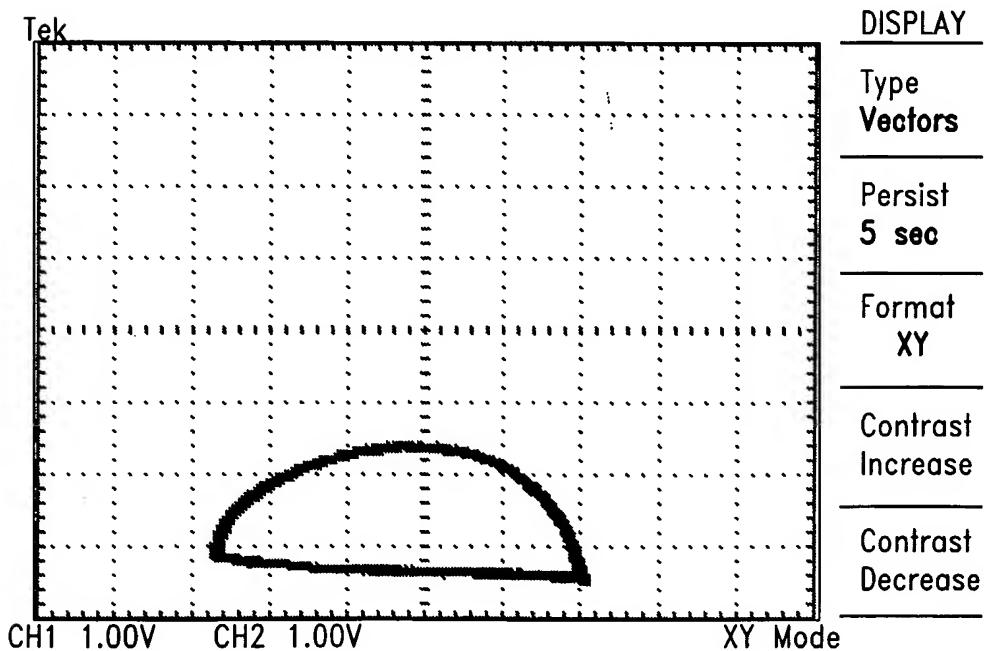


FIG. 19

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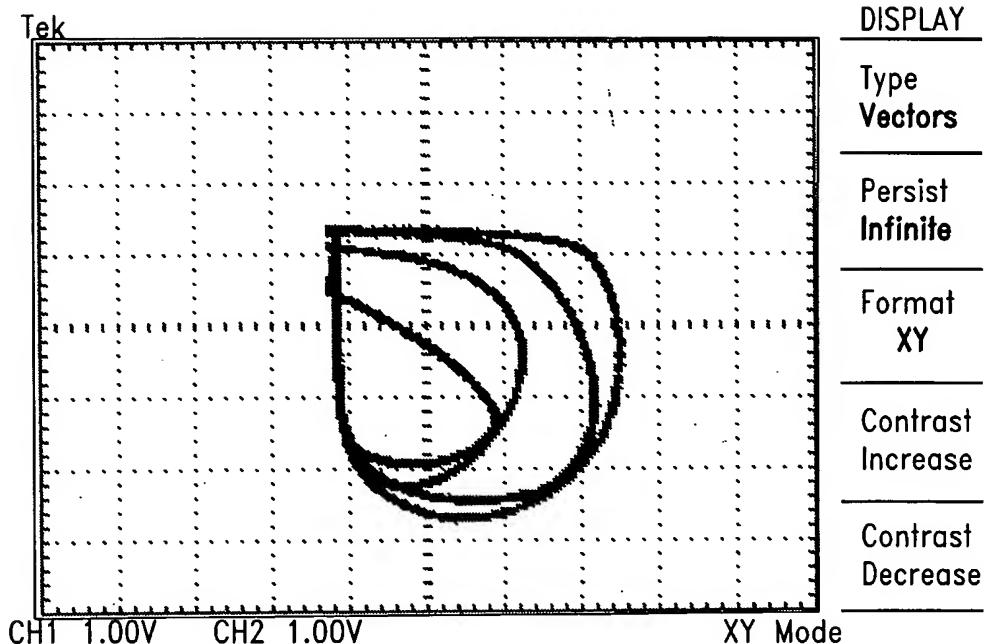


FIG. 20

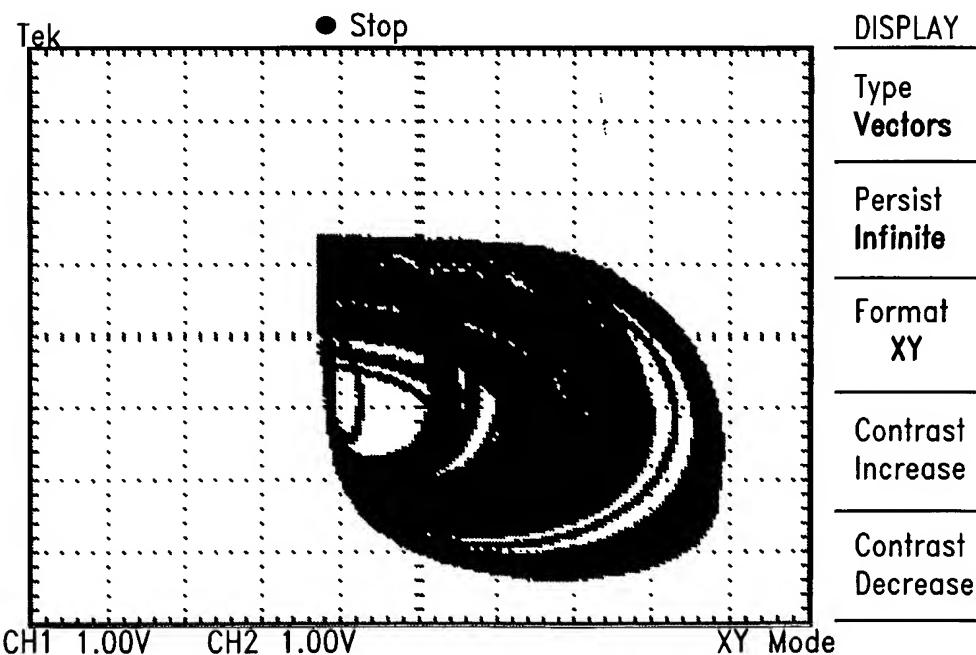


FIG. 21